**Task 1**: Fill in the boxes to complete the stages of the F-D-E cycle.

Fetch

Decode

Execute

**Task 2**: Label the diagram with the appropriate computer components and then explain the difference between the ADDRESS bus and the DATA bus.

RAM

CPU

Can I Have Some Data?

Yep! Here it is!

|  |  |
| --- | --- |
| **Address Bus** | Communicates the address of the memory location where data is to be fetched from. |
| **Data Bus** | Transfers data and instructions between the RAM and the CPU. |

**The Function of the CPU - ANSWERS**

**Task 3**: Label the various parts of the CPU and explain what each component is responsible for.

Control Unit (CU)

Immediate Access Store (IAS)

Arithmetic Logic Unit (ALU)

Main Memory (RAM)

Inputs & Outputs

**A**

**B**

**C**

|  |  |
| --- | --- |
| ***A:***  ***CONTROL UNIT*** | * It manages and monitors hardware on the computer to ensure the correct data goes to the correct hardware. * It manages the input and output signals ensuring these are dealt with correctly. * It manages the Fetch-Decode-Execute cycle. |
| ***B:***  ***IMMEDIATE ACCESS STORE*** | * Stores the data which is to be immediately processed… * …delivering the data to the ALU at speed. |
| ***C:***  ***ARITHMETIC LOGIC UNIT*** | * This is where the CPU actually carries out the maths and logic on the data (processes it).   It has two parts:   * Arithmetic part, which performs calculations on the data, e.g. 3 + 2 = 5 * Logic part – which deals with logical operations such as is True / False / Equal to / Greater than etc. |